REMARKS

Claims 1-24 remain pending. Claims 18 and 22 have been amended. No new matter has been added. Applicants understand new grounds of rejection have been presented.

Objections

The disclosure is objected to because of informalities as the Title of the instant application should be amended. Applicants respectfully disagree. Applicants point out that, for instance, the cover page of the specification, first page of the specification, abstract, transmittal, declaration and power of attorney are consistent in reciting the title as "A Request Tracking Data Prefetcher Apparatus." It appears to Applicants that the only inconsistency appears to be on the filing receipt from the Patent and Trademark Office. Accordingly, Applicants respectfully request the Examiner point out any other inconsistency or withdraw the rejection. In addition, Applicants will be filing a request for correction of the filing receipt.

Claims 18-20 and 22-24 are objected to as containing informalities. Applicants have herein amended independent Claims 18 and 22. Dependent Claims overcome the objections by virtue of their dependency. Accordingly, Applicants respectfully assert that the objections have been overcome.

35 U.S.C. Section 101 Rejections

Paragraph 5 of the above referenced Office Action rejects independent Claims 1-8 and 22-24 under 35 U.S.C. 101 because the claimed invention is directed to non-

statutory subject matter. Applicants respectfully disagree. Applicants point out that Claim 1 recites a request tracking data prefetch apparatus and further recites the limitations of a prefetcher and tracker coupled to a high latency memory as shown in Figures 1 and 3 (emphasis added). With regard to independent Claim 22, Applicants point out that Claim 22 recites a device for request tracking data prefetching for a computer system, as claimed (emphasis added). Further, Claim 22 recites a device comprising means for monitoring data transfers, means for using a bit vector to track multiple stream-type sequential processor access patterns, and a means for prefetching data, as claimed. Moreover, Applicants respectfully assert that Claims 1 and 22 satisfy the tied to a particular machine or apparatus criteria of In re Bilski, F.3d 943 (Fed Cir. 2008). Accordingly, Applicants respectfully assert that the claimed invention as recited in Claims 1-8 and 22-24 is directed to statutory subject matter and request withdrawal of the rejection.

35 U.S.C. Section 103(a) Rejections

Paragraph 3 of the above referenced Office Action rejects independent Claim 1 as being unpatentable over U.S. Patent No. 6,625,696 (hereinafter Willke), in further view of U.S. Patent No. 7,065,630 (hereinafter Ledebohm). As such, Applicants respectfully traverse and assert that the independent Claim 1 is not rendered obvious by Willke in view of Ledebohm. Applicants do not concede that Ledebohm is in fact prior art with respect to the instant application. Applicants reserve the right to antedate the Ledebohm references.

Applicants respectfully point out that the Examiner has the burden of establishing a prima facie case of obviousness. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations (emphasis added). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2100-126.

Applicants respectfully direct the Examiner to independent Claim 1 which recites in part (emphasis added):

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> a tracker within the prefetcher and configured to recognize processor accesses to a plurality of cache lines within a low latency memory operable to supply data to the processor responsive to processor data requests, wherein the processor accesses form a stream type sequential access pattern, and wherein further the tracker is configured to use a bit vector to predictively load a target cache line indicated by the stream-type sequential access pattern from the high latency memory into the low latency memory for the processor in preparation for the target cache line being requested by the processor as part of the stream-type processor access pattern.

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Independent Claim 9, 18, and 22 recite distinguishing limitations similar to those recited in Claim 1.

The rejection admits that Willke does not specifically teach the requesting device is a processor except that the requesting device is peripheral device. The rejection relies

on Ledebohm as teaching a peripheral device in a computer system wherein the peripheral device is a graphics processor. To the contrary, Applicants respectfully disagree and respectfully assert that Ledebohm does not remedy the shortcomings of Willke. Applicants point out that Claim 1 recites the limitations of recognizing processor accesses to a plurality of cache lines, as claimed (emphasis added). Applicants understand Ledebohm to mention a selected portion of the memory of a peripheral device can be mapped to virtual memory at any time in response to a request from a device driver program or other process, enabling direct CPU access to the mapped portions of the peripheral memory (Col. 3, lines 43-47). To the extent that Ledebohm may mention a graphics processing unit (Figure 1 and Col. 4, lines 4-6), Applicants respectfully assert that Ledebohm is silent as to recognizing processor accesses to a plurality of caches lines, as claimed. Further, Applicants respectfully assert that because Ledebohm fails to teach recognizing accesses to a plurality of caches lines, Ledebohm cannot teach or suggest the limitations of recognizing accesses to a plurality of caches lines within a low latency memory operable to supply data to the processor responsive to processor data requests, as claimed (emphasis added). Accordingly, Applicants respectfully assert that the cited references fail to render obvious embodiments of the present invention as recited in Claim 1 within the meaning of 35 U.S.C. §103(a).

Independent Claims 9, 18, and 22 are patentable for similar reasons. All related dependent claims are patentable at least by virtue of their dependency.

The above referenced Office Action also rejects Claim 17 under 35 U.S.C. 103(a) as being unpatentable over Willke, in view of Ledebohm, further in view of Microsoft

Computer Dictionary (hereinafter "Microsoft"). Applicants respectfully disagree. Applicants do not concede that Ledebohm is in fact prior art with respect to the instant application. Applicants reserve the right to antedate the Ledebohm reference. For the reasons stated above, Applicants respectfully submit that independent Claim 9, from which Claim 17 depends is allowable over Willke and Ledebohm. In addition, Applicants respectfully submit that Microsoft does not remedy the shortcomings of Willke and Ledebohm in that Microsoft fails to teach or suggest the limitations of recognizing accesses to a plurality of caches lines within a low latency memory operable to supply data to the processor responsive to processor data requests, as claimed. Therefore, Applicants respectfully assert that the embodiments of the present invention as recited in Claim 17 are not rendered obvious by the combination of Willke, Ledebohm, and Microsoft within the meaning of 35 U.S.C. 103(a).

The above referenced Office Action rejects Claims 19, 20, and 23 under 35 U.S.C. 103(a) as being unpatentable over Willke in view of Ledebohm, further in view of Brooks (US 6,081,868). Applicants respectfully disagree. Applicants do not concede that Ledebohm is in fact prior art with respect to the instant application. Applicants reserve the right to antedate the Ledebohm reference. For the reasons stated above, Applicant respectfully submits that independent Claim 18, from which Claims 19 and 20 depend, independent Claim 22, from which Claims 23 depends, are allowable over Willke and Ledebohm. In addition, Applicants respectfully submit that Brooks does not remedy the shortcomings of Willke and Ledebohm in that Brooks fails to teach or suggest the limitations of recognizing accesses to a plurality of caches lines within a low latency memory operable to supply data to the processor responsive to processor data

requests, as claimed. Therefore, Applicants respectfully assert that the embodiments of the present invention as recited in Claims 19, 20, and 23 are not rendered obvious by the combination of Willke, Ledebohm, and Brooks within the meaning of 35 U.S.C. 103(a).

CONCLUSION

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
MURABITO, HAO & BARNES

Dated: 12/1, 2009

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